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JAY CHESAVAGE 3833 MIDDLEFIELD PALO ALTO, CA 94303			EXAMINER WONG, WARNER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/804,349

Applicant(s)

BECHTOLSHEIM ET AL.

Examiner

Warner Wong

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 73-119 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 73-119 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Objections

1. Claims 75-83 are objected to because of the following informalities: each claim describes that "final data compris[ing] n data lanes". It is understood that "data" itself cannot comprise (include) data lane(s); only data lane(s) can comprise/include "data". Each of such descriptions needs to be grammatically rewritten.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 73-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant (US 6,081,523) in view of Shimizu (US 5,293,378).

Regarding claim 73, Merchant describes a communication interface comprising n data lanes (abstract & fig. 1, data lanes 22[0] to 22[n]), said interface sequentially transmitting a header distributed across a plurality of said data lanes (fig. 3A & col. 6, lines 13-16, preamble+start frame delimiter (header) sent on each MII 28i), a variable amount of payload data distributed across a plurality of said n data lanes (fig. 3A & col. 6, lines 18-24, segmented Ethernet (variable) data streams N0-N3 distributed across the links);

said header includes transmitting a START symbol on first said data lane, and the transmission of said payload data is followed by an CRC symbol on at least one said data line (fig. 3A & col. 6, lines 50-55, preamble (header) comprising start frame delimiter (col. 6, lines 13-15), followed by payload data, then a CRC symbol);

said payload data includes transmitting data across said n data lanes up to data lane m, where $m \leq n$ and $n > 1$ (fig. 1, transmitting across $n=4$ data lanes, 22[0]-22[4]).

Merchant describe that the CRC field is generated lastly after the preamble and data, but fails to explicitly state that the CRC symbol being an END symbol.

Shimizu explicitly describe sending an END symbol fig. 2, transmitting End Delimiter ED on said lane 102).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to describe sending an end symbol as in Shimizu for the invention of Merchant.

The motivation for combining the teachings is that it allow for a separating means for the transmission using such a delimiter (Shimizu, col. 2, lines 6-7).

Regarding claim 74, Messenger further describes that $n=4$ (fig. 1).

4. Claim 75-76, 78, 80, 82-83 and 86-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu in view Finney (US 5,570,356).

Regarding claim 75, Shimizu describes a process for transmitting data on a communications channel said data comprising a header and a variable length payload (col. 1, lines 19-21, may be Ethernet-based packets, with header and payload), the

channel having a first, a second, a third, and a fourth data lane (fig. 1, transmission lines 5-8), said process comprising:

a first step of sending a synchronization symbol on all four said data lanes for a synchronization interval, or until said variable length payload is ready to be transmitted (fig. 2, sending SYN on all 4 paths/lanes before the transmission frame (sync interval));

a second step of substantially simultaneously sending said header to said first data lane and part of said payload to the remaining three data lanes (fig. 2, col. 4, lines 20-26, parallel transmitting the start delimiter SD, and segments a-d in the first frame cycle);

a third step of incrementally transmitting the remainder of said payload data in a sequence of transmission events (fig. 2, incrementally transmitting segment 'e'), each said transmission event comprising substantially simultaneously sending said incremental payload data in said four data lanes until final data comprising one data lanes of said payload data remains to be transmitted (fig. 22, sending until last segment 'f' on lane 102 (one lane));

a fourth step of transmitting said final data accompanied by an END symbol on one said data lane (fig. 2, transmitting End Delimiter ED on said lane 102).

Shimizu fails to explicitly describe that each data lane being 8 bits wide as in applicant fig. 16, intermediate stage 8-bit lanes.

Finney describes a transmitting method when each data lane from the collective set of MUXes 230, 232 & 234 are 8-bits wide (fig. 2 & col. 4, lines 16-19: "wherein a

standard Widmer et al. 8-bit/10-bit encoding is performed to provide a data string of 10 encoded bits for each 8-bit byte to serializers 246, 248 & 250").

Shimizu also fails to describe that the process includes a clock for transferring said 8-bits.

Finney describe that the process includes a clock for transferring said 8-bits (fig. 4, clock for pacing transmission clock cycles).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to describe the details to parallel transmission of Messenger to have the 8B/10B encoding means as in Finney.

The motivation for combining the teachings is that it enables a high bandwidth communication protocol for transmission using multiple serial data links (Finney, col. 2, lines 12-14).

Regarding claim 76, Shimizu further suggests that the final data comprises zero said data lanes and said END symbol is transmitted on said first data lane (fig. 2, col. 4, lines 26-28, should segment 'f' is transmitted in path 104 in the entire second frame cycle, 'ED' (END symbol) is then transmitted on path 101 (first data lane)).

Regarding claim 78, Shimizu further suggests: the final data comprises first said data lane and said END symbol is transmitted on said second data lane (fig. 2, segment 'e' may be the last segment in which the ED end delimiter is transmitted on the second data lane).

Regarding claim 80, Shimizu further suggests: the final data comprises first and second said data lanes and said END symbol is transmitted on said third data lane (fig.

2, segment 'e' & 'f' are the last segments (final data), where segment 'f' may span the entire payload of the second data lane in which the ED end delimiter is transmitted on the third data lane).

Regarding claim 82, Shimizu further suggests: the final data comprises first, second and third said data lanes and said END symbol is transmitted on said fourth data lane (fig. 2, last segments may span the entire payload of lanes 101, 102 & 103 in which the ED end delimiter is transmitted on the fourth data lane).

Regarding claim 83, Shimizu further suggests: the final data comprises first, second and third said data lanes and said END symbol is transmitted on said fourth data lane (fig. 2, last segments may span the entire payload of lanes 101, 102 & 103 in which the ED end delimiter is transmitted on the fourth data lane).

Regarding claim 86, Shimizu and Finney combined describe using a positive edge for data transfer (Finney, fig. 4, rising/positive edge of clock for pacing phases 1-3) using a clock with lower frequencies (col. 2, lines 20-21), but not specifically at 312.5Mhz rate.

However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the transmission clock rate or frequency of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on the Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In

re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Thus, it would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify the transmission clock rate to 312.5Mhz for the claim limitation since it is generally considered to be within the ordinary skill in the art to adjust, vary select or optimize the transmission clock rate/frequencies.

Regarding claim 87, Shimizu and Finney combined describe: each data lane is encoded and serialized into a serial stream of data (Finney, fig. 2, data stream encoded at 236, 238 & 240 and serialized at 246, 248 & 250 for transmission).

Regarding claim 88, Shimizu, Finney and Cam combined describe: said encoder is an 8B/10B encoder (fig. 2 236,238,240 & col. 4, line 17).

Regarding claim 89, Shimizu further suggests that the serial stream of data is transmitted as a differential electrical signal (col. 1, lines 9-11, telephone line or twisted-pair cable as the transmission medium).

5. Claim 77, 79 and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu in view of Finney as applied to claim 75 above, and further in view of Merchant.

Regarding claim 77, Shimizu fails to describe: final data comprises zero said data lanes and said END symbol is transmitted on said first data lane accompanied by said preamble transmitted on said second, said third and said fourth data lanes.

Merchant describes that last data segment (final data) ends at the fourth/last data lane MII 28[3], the CRC (END) symbol is transmitted on the first data lane MII 28[0], and the preamble is also transmitted on the second, third and fourth data lane (fig. 3A).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to describe such transmission specifics for the preamble, final data and the END symbol as in Merchant for the combined parallel transmission of Shimizu and Finney.

The motivation for combining the teachings is that such transmission configuration increases the effective transmission data rate (Merchant, col. 2, lines 2-6).

Regarding claim 79, Shimizu further suggests: final data comprises first said data lane and said END symbol is transmitted on said second data lane accompanied by said preamble transmitted on said third and said fourth data lanes (fig. 2, segment 'e' may be the last segment in which the ED end delimiter is transmitted on the second data lane).

Shimizu fails to describe that the preamble is transmitted on said third & fourth data lanes.

Merchant describes that the preamble is transmitted on said third & fourth data lanes.

Regarding claim 81, Shimizu describes: the final data comprises said first and said second data lanes and said END symbol is transmitted on said third data lane (fig. 2, segment 'e' & 'f' are the last segments (final data), where segment 'f' may span the

entire payload of the second data lane in which the ED end delimiter is transmitted on the third data lane).

Shimizu fails to describe: the preamble transmitted on said fourth data lane.

Merchant describes that the preamble is transmitted on said fourth data lane. third data lane).

6. Claims 84-85 and 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu in view of Finney as applied to claim 75 above, and further in view of Kimmitt (US Kimmitt US 6,618,395).

Regarding claim 84, Shimizu and Finney combined describe transmission using a clock with lower frequencies (Finney fig. 6 & col. 2, lines 20-21), but not specifically at 312.5Mhz rate.

Kimmitt describes a plural channel transmission method where each path uses 156.25Mhz.

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to describe using a 156.25Mhz clock rate as in Kimmitt for the combined transmission of Shimizu and Finney.

The motivation for combining the teachings is that allows for a reliable telecommunications without employing wide parallel buses (Kimmitt, col. 2, lines 4-9).

Regarding claim 85, Shimizu and Finney combined describe using a positive edge (Finney, fig. 4, rising/positive edge of clock for pacing phases 1-3) and a negative edge (Finney, fig. 4, falling/negative edge of phase 1 for gating data to register),

clocking at lower frequencies (Finney fig. 6 & col. 2, lines 20-21), but fails to describe using a clock rate of 156.25Mhz.

Kimmitt describes using a clock rate of 156.25Mhz for transmission (col. 7, lines 59-65).

Regarding claim 90, Shimizu, Finney and Cam combined fail to describe data transmission as an optical signal.

Kimmitt describe that the multi-channel data transmission using an optical signal (col. 4, lines 22-23).

7. Claim 91 is rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu.

Regarding claim 91, Shimizu describes a transmitter (fig. 1, transmitter 16) for sending data comprising a header followed by a variable length payload (col. 1, line 20, can be for ethernet frame comprising header & variable payload) , said data being substantially simultaneously transmitted on a first data lane, a second data lane, a third data lane and a fourth data lane in a succession of time sequences (fig. 2, segments a-d simultaneously, then e-f successively), wherein said variable length data is incrementally transmitted on said first, said second, said third, and said fourth data lanes during each said time sequence in the following manner:

sending a preamble on said first, said second, said third, and said fourth data lanes until said variable length data is ready to transmit (fig. 2, SYN (preamble) is sent on paths 101-104 before packet), and when said data is ready to transmit:

sending a START symbol on said first data lane and said variable length data on said second, said third, and said fourth data lanes during one said time sequence (fig. 2, SD sent on lane 101 & data b,c,d sent on lanes 102-104 during the same time cycle);

sending the remainder of said variable length payload on said first, said second, said third, and said fourth data lanes during successive said time sequence until there is insufficient data to send on all four said data lanes, said insufficient data being final data (fig. 2, sending until (final) data e & f);

where there is no said final data to send, sending said END symbol on said first lane (fig. 2; payload info may be shorter than specify drawing where last segment (final data) is 'e' and the ED (END symbol) is included in path/lane 101, and said preamble on said second, said third, and said fourth lanes (fig. 2, SYN's are sent on paths 102-104 afterwards);

when said final data comprises one said data lane, sending said final data on said first lane, an END symbol on said second lane, and said preamble on said third and fourth lanes (fig. 2, last segments may span entire paths/lane 101 where ED (END symbol) is sent on lane 102 and SYN (preambles are sent on lanes 103-104 thereafter);

when said final data comprises two said data lanes, sending said final data on said first lane, an END symbol on said second lane, and said preamble on said third and said fourth lanes (fig. 2, last segments (final data) 'e' and 'f' on lanes 101 & 102, ED on lane 102, and SYN (preamble) are also sent on paths/lanes 103 & 104);

when said final data comprises three said data lanes, sending said final data on said first, said second, and said third lane, an end symbol on said fourth lane (fig. 2, last

segments may span entire paths/lanes 101-103 where ED (END symbol) is sent on lane 104);

8. **Claim 92-93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu as applied to claim 91 above, and further in view of Finney.

Regarding claim 92, Shimizu fails to describe that the data lane is 8 bits wide.

Finney describes that the data lane is 8 bits wide (fig. 2 & col. 4, lines 15-20, 8-bit wide lane input to 8B/10B encoder).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to describe the details to parallel transmission of Messenger to have the 8-bit wide data lane for 8B/10B encoding as in Finney.

The motivation for combining the teachings is that it enables a high bandwidth communication protocol for transmission using multiple serial data links (Finney, col. 2, lines 12-14).

Regarding claim 93, Shimizu and Finney combined describe that each MII path use is 8-bits wide ((fig. 2 & col. 4, lines 15-20, 8-bit wide lane input to 8B/10B encoder) and transmission using a clock with lower frequencies (Finney, fig. 6 & col. 2, lines 20-21), but not specifically at 312.5Mhz rate.

However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the transmission clock rate or frequency of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on the Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937);

Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Thus, it would have been obvious to one with ordinary skill in the art at the time of invention by applicant to modify the transmission clock rate to 312.5Mhz for the claim limitation since it is generally considered to be within the ordinary skill in the art to adjust, vary select or optimize the transmission clock rate/frequencies.

Claims 94, 95, 96 and 98 have the same limitations as claims 85, 86, 87 and 88 respectively and therefore are rejected under the same rationale.

Regarding claim 99, Shimizu further suggests: each said data lane comprises 8 bits of data and one bit of clock (abstract & fig. 2, data in each channel is sent in bytes (8-bits) and the SYN marker may be sent in 1-bit).

9. **Claim 97** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu and Finney as applied to claim 96 above, and further in view of Widmer (US 6,496,540).

Finney suggests that each said data lane includes an encoder (col. 2, lines 37-44, transmitting means have encoding since receiving means have decoding) and encoding for transmission using a clock with lower frequencies (Finney fig. 6 & col. 2, lines 20-21), but not specifically at 312.5Mhz rate.

However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the transmission clock rate or frequency of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on the Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Thus, it would have been obvious to one with ordinary skill in the art at the time of invention by applicant to modify the transmission clock rate to 312.5Mhz for the claim limitation since it is generally considered to be within the ordinary skill in the art to adjust, vary select or optimize the transmission clock rate/frequencies.

Finney also fails to describe: each serializer is clocked at 10 times said encoder clock rate.

Widmer describes as a prior art it is conventional to serialize at a rate of 10 times the parallel encoded rate for transmission (col. 1, lines 34-37 & 41).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to specify that the serializer uses a rate of 10 times of said encoder clock rate in the transmitter as in Widmer for the transmitter of Finney.

The motivation for combining the teachings is that it allows a higher transmission rate (Widmer, col. 1, lines 31-32).

10. **Claims 100 & 101** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu and Finney as applied to claim 93 above, and further in view of Chung (US 5,764,895).

Shimizu and Finney combined fail to describe: data from each data lane is transmitted least/most significant bit (MSB/LSB) first and most/least significant bit last.

Chung describes as a prior art that in parallel transmissions, data from each data lane can be transmitted in big-endian or little-endian ordering (MSB/LSB transmission) (col. 2, lines 8-11).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify a MSB/LSB transmission ordering as in Chung for the parallel transmission in Shimizu and Finney.

The motivation for combining the teachings is that it would allow flexibility/compatibility for interconnecting with the target of the network.

11. **Claim 102-103** are rejected under 35 U.S.C. 103(a) as being unpatentable over Finney in view of Widmer (US 6,496,540).

Regarding claim 102, Finney describes a transmitter (fig. 2) for generating streams of serial data, said transmitter including:

a transmit buffer (fig. 2, registers 202,204,206) for receiving 24 bits of data (3-bytes) and separating said 24 bits of data into three data lanes, each data lanes comprising 8 bits (1-byte) of data (fig. 2 & col. 2, lines 24-26) and a clock (fig. 4, clock),

each data lane having:

an encoder for converting said 8 bits of data accompanied by said clock into 10 bits of encoded data (fig. 2 & col. 4, lines 15-18);

a serializer for transmitting said 10 bits of encoded data into a stream of serial data (fig. 2, serializer 246).

Although Finney exemplified splitting and transmitting 24 bits/3-bytes over three data lanes, his invention is generally described for (other) multiple serial transmissions (col. 2, lines 24-26).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to understand and apply his concept to specifically be used for 4-bytes over four data lanes serial transmission.

Finney describes transmission using a clock with lower frequencies (Finney, fig. 6 & col. 2, lines 20-21), but not specifically at 312.5Mhz rate.

However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the transmission clock rate or frequency of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on the Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Thus, it would have been obvious to one with ordinary skill in the art at the time of invention by applicant to modify the transmission clock rate to 312.5Mhz for the claim limitation since it is generally considered to be within the ordinary skill in the art to adjust, vary select or optimize the transmission clock rate/frequencies.

Finney describes that the fast transmission rate received by its receiver's serializer will be handled at a lower clocking frequencies afterwards, but fails to describe that the serializer is clocked at 10 times said encoder clock rate.

Widmer describes as a prior art it is conventional to serialize at a rate of 10 times the parallel encoded rate for transmission (col. 1, lines 34-37 & 41).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to specify that the serializer uses a rate of 10 times of said encoder clock rate in the transmitter as in Widmer for the transmitter of Finney.

The motivation for combining the teachings is that it allows a higher transmission rate (Widmer, col. 1, lines 31-32).

Regarding claim 103, Finney exemplifies a receiver (fig. 6) for converting streams of serial data into a series of 24 bit words, the receiver having:

three input data processors (fig. 3 receiver chip), each said data processor having:

a deserializer for converting a stream of serial data into said 10 bits of parallel encoded data (fig. 6, deserializers 602,604,606 outputting 10 bits for 10B/8B decoders) and a clock (fig. 4, clock);

a decoder for converting said 10 bits of parallel encoded data into 8 bits of decoded data (fig. 6, 10B/8B decoders 642,644,646);

a transmit buffer coupled to each said decoder and each said clock, said transmit buffer (fig. 6, registers 642,644,646);

Although Finney exemplified receiving and combining 24 bits/3-bytes over three data lanes, his invention is generally described for (other) multiple serial transmissions (col. 2, lines 24-26).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to understand and apply his concept to specifically be used for 4-bytes over four data lanes serial transmission.

Finney describes transmission using a clock with lower frequencies (Finney, fig. 6 & col. 2, lines 20-21), but not specifically at 312.5Mhz rate.

However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the transmission clock rate or frequency of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on the Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Thus, it would have been obvious to one with ordinary skill in the art at the time

of invention by applicant to modify the transmission clock rate to 312.5Mhz for the claim limitation since it is generally considered to be within the ordinary skill in the art to adjust, vary select or optimize the transmission clock rate/frequencies.

Finney fails to describe that the deserializer is clocked at 10 times said decoder clock rate for a 3.125Ghz serial stream.

Widmer describes as a prior art it is conventional to deserialize at a rate of 10 times the parallel encoded transmission rate (col. 1, lines 34-37 & 41).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to specify that the deserializer uses a rate of 10 times of said encoder clock rate in the transmitter as in Widmer for the transmitter of Finney for a 3.125Ghz rate transmitted stream.

The motivation for combining the teachings is that it allows a higher transmission rate (Widmer, col. 1, lines 31-32).

12. Claims 104-105 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finney.

Regarding claim 104, Finney exemplifies a receiver (fig. 6) for converting streams of serial data into a variable length data payload (col. 5, lines 16-19, receiving variable length frames), said receiver comprising:

deserializers each coupled to a respective serial stream (fig. 6, deserializers 602,604,606) , each said deserializer converting said stream of serial data into 10 bits of

encoded data (fig. 8, output is 10 bits for the 10B/8B decoder), accompanied by a clock for each said serial stream (fig. 8 & col. 5, lines 38-40, clock used by each deserializer);

decoders, each said decoder coupled to a respective said deserializer output each said decoder converting each said 10 bits of encoded data into 8 bits of decoded data (fig. 6, the connecting 10B/8B decoders 622,624,626), thereby producing 8 bits of encoded data accompanied by a clock (fig. 8 & col. 5, lines 47-54, clock used to shift the output 8 bits from the 10B/8B decoder into registers 632,634,636);

an elasticity buffer coupled to each said 8 bit decoder data and decoder clock (fig. 6, registers 632,634,636,642,644,646), and combining said 32 bits of data over successive intervals to produce said variable length packet.

Although Finney exemplified receiving and combining 24 bits/3-bytes over three data lanes, his invention is generally described for (other) multiple serial transmissions (col. 2, lines 24-26).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to understand and apply his concept to specifically be used for 4-bytes over four data lanes with 4 deserializers and 4 decoders.

Finney describe that each path and its buffer use a clock with lower frequencies (Finney, fig. 6 & col. 2, lines 20-21), but not at 312.5Mhz rate.

However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the transmission clock rate or frequency of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on the Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937);

Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Thus, it would have been obvious to one with ordinary skill in the art at the time of invention by applicant to modify the transmission clock rate to 312.5Mhz for the claim limitation since it is generally considered to be within the ordinary skill in the art to adjust, vary select or optimize the transmission clock rate/frequencies.

Regarding claim 105, Finney further describes that the decoder is an 8B/10B decoder (fig. 6, 622,624,626).

13. Claims 106-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finney as applied to claim 104 above, and further in view of Shimizu.

Regarding claim 106, Finney fails to describe:

said variable length payload is formed using data received on the other three said decoders following a START symbol on one said decoder, thereafter using data from all four said decoders until receipt of an END symbol on any said decoder.

Shimizu describes:

said variable length payload is formed using data received on the other three said decoders following a START symbol on one said decoder, thereafter using data from all four said decoders until receipt of an END symbol on any said decoder (abstract

& fig. 2, SD (START symbol) and ED (end symbol) at the decoders of the receiving means, col. 2, lines 41-45).

It would have been obvious to one with ordinary skill in the art at the time of invention to specify a START and an end symbol in receiving the variable length payload at one of the 4 receiver decoding paths as in Shimizu for the parallel transmission path of Finney.

The motivation for combining the teachings is that packets can be transmitted at a high rate over a long transmission distance using a transmission medium which is economical and easy to handle (Shimizu, col. 2, lines 47-50).

Regarding claim 107, Finney fails to describe:

said variable length payload is formed using data between a START symbol on one said decoder and an END symbol received on any said decoder.

Shimizu describes:

said variable length payload is formed using data between a START symbol on one said decoder and an END symbol received on any said decoder (abstract & fig. 2, SD (START symbol) and ED (end symbol) at the decoders of the receiving means, col. 2, lines 41-45).

Regarding claim 108, Finney further describes:

said elasticity buffer forms said variable length payload by concatenating data received from a first decoder, a second decoder, a third decoder, and a fourth decoder (fig. 6 and col. 5, lines 60-67, registers 642,644,646 (buffer) concatenates data output from decoders 622,624,626, see fig. 7: concatenated data in the word synch stage).

Finney fails to describe a START symbol is received on a first decoder and said variable length packet is formed from concatenating said data in sequence from said second decoder, said third decoder, said fourth decoder, and said first decoder, repeating until terminated by the receipt of an END symbol on any decoder.

Shimizu describes: a START symbol is received on a first decoder and said variable length packet is formed from concatenating said data in sequence from said second decoder, said third decoder, said fourth decoder, and said first decoder, repeating until terminated by the receipt of an END symbol on any decoder (abstract & fig. 2, SD (START symbol) and ED (end symbol) at the decoders of the receiving means, col. 2, lines 41-45).

14. **Claims 109-111** are rejected under 35 U.S.C. 103(a) as being unpatentable over Finney as applied to claim 104 above, and further in view of Kimmitt.

Regarding claim 109-110, Finney fails to describe that each said serial stream of data is derived from a differential electrical signal or an optical signal.

Kimmitt describes that each said serial stream of data is derived from a differential electrical signal or an optical signal (col. 4, lines 22-24).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to explicitly describe copper or fiber optics for transmission of Shimizu and Finney.

The motivation for combining the teachings is that allows for a reliable telecommunications without employing wide parallel buses (Kimmitt, col. 2, lines 4-9).

Regarding claim 111, Finney describe using a positive edge (Finney, fig. 4, rising/positive edge of clock for pacing phases 1-3) and a negative edge (Finney, fig. 4, falling/negative edge of phase 1 for gating data to register), clocking at lower frequencies (Finney fig. 6 & col. 2, lines 20-21), but fails to describe using a clock rate of 156.25Mhz.

Kimmitt describes using a clock rate of 156.25Mhz for transmission (col. 7, lines 59-65).

Independent claim 112 is a process claim which closely describes all features recited in the receiver claims 104 and 106 combined and thus rejected using the same rationale.

Claims 113, 117, 118 and 119 recites the same features as claims 105, 111, 109 and 110 respectively and therefore are rejected using the same rationale.

Claim 114 recites the same claim features embedded in claim 104 and is thus rejected under the same rationale.

Claim 115 recites the same claim features in claim 102 and is thus additionally rejected under the same rationale.

Claim 116 recites the same claim features in claim 95 and is thus additionally rejected under the same rationale.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hendel (US 6,591,303) describing parallel trunking, Harriman (US 5,561,771) describing transmission using subsets of bus lines, Kinami (US 5,317,415) describing a data communication method using a plurality of lines, Dretzka (US 4,703,475) describing data communication using multiple physical data links and Krishna (US 6,094,439) describing a multiple physical link arrangement.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 6:30AM - 3:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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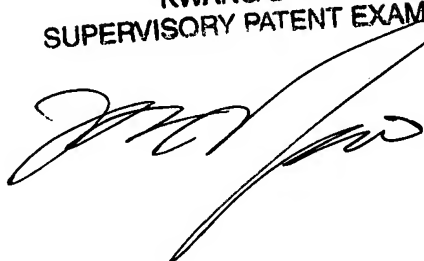
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Warner Wong
Examiner
Art Unit 2616

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KWANG BIN YAO
SUPERVISORY PATENT EXAMINER

A handwritten signature in black ink, appearing to be 'K. B. Yao', written over the printed name and title.